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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,549	01/18/2000	Korbin Van Dyke	01000.9901080	9816

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/484,549	DYKE ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 – 12, 16 - 18 and 20 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 – 12, 16 - 18 and 20 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2 – 12, 16 - 18 and 20 - 23 are presented for examination. Claims 1, 13 – 15 and 19 have been cancelled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 – 12, 16, 18, 20 - 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "the resources" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 16, line 8 and **claim 18**, line 4 detail "the tasks" does this correspond to the "queued task" or are these different tasks. If it's the same tasks restate as "the queued tasks".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 – 12, 16, 17, 18, 20 - 23 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharrit et al. (US Pat. 5,999,990, hereinafter Sharrit) in view of Bonola (US Pat. 5,706,514).

6. As per **claims 16 and 18**, Sharrit teaches the invention as claimed, including a method for providing multimedia functionality comprising:

keeping track, remotely from the resources, of the capabilities of all available processors in a homogeneous multiprocessors environment in the integrated circuit, wherein each of the available processors in the integrated circuit is operatively coupled to a bus in the integrated circuit (fig. 1, col. 3 lines 14 – 55, col. 5 lines 32 – 57);

identifying, independent of the tasks, available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (col. 3 lines 14 - 55);

allocating available processing resources in the homogeneous multiprocessor environment independent of the tasks (col. 3 lines 14 - 55);

allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment and the processing requirements of each of the tasks (col. 3 lines 14 - 55);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 5 lines 17 – 32, col. 7 lines 14 - 55, col. 9 lines 4 - 20 and fig. 6); and

performing the tasks using the available processing resources to produce resulting data, wherein the functional programs cause the available processing resources to perform the tasks of at least one of: graphics image processing, video processing, audio processing and communications processing (col. 1 lines 56 - 59, col. 2 lines 18 – 21, col. 3 lines 50 – 55, col. 4 lines 9 – 18, col. 5 lines 2 - 16).

Sharrit discloses that a plurality of processing tasks to be supported by the communicator are identified (col. 10 lines 3 -8) but did not clearly disclose the tasks are being queuing. Nevertheless, Bonola discloses the step of queuing the tasks to be processed in a homogeneous environment (col. 3 lines 61 – 65). It would have been obvious to one of an ordinary skill in the art, at the time the invention was made to incorporate the features as disclosed by Bonola together with Sharrit for queuing the tasks to be processed according to their priority assignment (Sharrit: col. 10 lines 5 - 8).

7. As per **claim 2**, as modified Sharrit teaches the invention as claimed, including the method of claim 18 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (Sharrit: col. 1 line 50 – col. 2 line 3, col. 5 line 33 – col. 6 line 41. Bonola: col. 2 lines 6-10; col. 3 lines 37-44).

8. As per **claim 3**, as modified Sharrit teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit

pattern but perform different operations (Sharrit: col. 5 line 33 - col. 6 line 41. Bonola: col. 1 lines 15 – 26, col. 2 lines 6 – 10 and col. 3 lines 37 - 44).

9. As per **claim 4**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (Sharrit: col. 2 lines 51 – 58, col. 5 line 33 – col. 6 line 41. Bonola: col. 3 lines 26-35; col. 7 lines 22-33).

10. As per **claim 5**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (Sharrit: col. 4 line 3 -8, 48 – 60. Bonola; col. 8 lines 31-45).

11. As per **claim 6**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise x86 processing (Sharrit: col. 1 lines 55 – 61, col. 2 lines 18 – 21. Bonola: col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

12. As per **claim 7**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 further comprising:

receiving the initial data from a first input/output device (Sharrit: col. 5 lines 17 – 32. Bonola: col. 8 lines 11-15).

13. As per **claim 8**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 further comprises:

passing the resulting data to a first input/output device (Sharrit: col. 5 lines 3 – 32. Bonola: col. 9 lines 13-23).

14. As per **claim 9**, as modified Sharrit teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (Sharrit: col. 2 lines 51 – 58, col. 5 lines 3 – 17 and fig. 1. Bonola: col. 9 lines 13-23).

15. As per **claim 10**, as modified Sharrit teaches the invention as claimed, including the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (Sharrit: col. 7 lines 14 – 44. Bonola: col. 8 lines 46-65).

16. As per **claim 11**, as modified Sharrit teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (Sharrit: col. 3 lines 51 – col. 4 lines 18, col. 5 lines 3 - 17. Bonola: col. 9 lines 13-15, 19-23).

17. As per **claim 12**, as modified Sharrit teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (Sharrit: col. 1 lines 59 - 64, col. 7 lines 14 -44. Bonola: col. 8 lines 46-65).

18. As per **claims 17 and 23**, Sharrit teaches the invention as claimed, including an apparatus comprising:

a plurality of homogeneous processors in an integrated circuit coupled to a bus in the integrated circuit (fig. 1, col. 15 line 32 - 57);

an input/output interface coupled to the bus (fig. 1);

an input/output device coupled to the input/output interface, the plurality of processors processing program code configured to perform a plurality of tasks (fig. 1, col. 3 line 51 – col. 4 line 25, col. 4 lines 58 – 60, col. 5 line 28 – col. 6 line 13), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with an input/output device (col. 7 lines 14 - 55);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 7 lines 27 - 44);

wherein the first portion of the plurality of processors provides functionality as found in an application-specific subsystem and wherein the input/output device is the application-specific subsystem (col. 3 line 51 – col. 4 line 3, col. 5 lines 17 - 32); and

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode (col. 7 lines 14 - 44).

Sharrit discloses that his system is capable of being configured to cause a portion of the plurality of processors to perform any of a variety of processing tasks (col. 1 lines 56 – 59) but did not clearly discloses his system is coupled to a plurality of input/output devices. Nevertheless, Bonola discloses that his system comprises a plurality of i/o devices and that I/O devices are being allocated to slave computers (figs. 1 and 2, col. 5 lines 31 – 47, col. 4 lines 52 – 57, col. 8 lines 11-15, col. 9 lines 13 – 27, col. 7 lines 22-25, 42 – 52).
Therefore, it would have been obvious to one of an ordinary skill in the art, at the time the invention was made to combine Bonola's teaching together with Sharrit to entail enable/disable the I/O devices and their connection to the processor for task execution.

19. Regarding **claims 20 and 21**, as modified Sharrit discloses the step of allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment comprises allocating the available

processing resources among the tasks based on the ability of each of the available processors of the homogeneous multiprocessor environment to be aggregated with another processor to provide a processing resource (Sharrit: col. 9 lines 4 – 20, col. 8 lines 28 – 40).

20. Regarding **claim 22**, as modified Sharrit discloses providing to the available processing resources functional programs corresponding to the tasks comprises providing to the available processing resources functional programs and initial data corresponding to the tasks (Sharrit: fig. 6, col. 7 lines 14 – 55, col. 9 lines 4 – 20).

Response to Arguments

21. Applicant's arguments with respect to claims 16, 17, 18 and 20 - 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lilian Vo
Examiner
Art Unit 2195

lv
January 31, 2008

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER